

**TITLE: PIPELINE ARCHITECTURE FOR MULTI-SLOT WIRELESS LINK
PROCESSING**

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SPECIFICATION

Cross References to Related Applications

This application claims priority to U.S. Provisional Patent Application Serial No. 60/431,940, filed December 9, 2002, and to U.S. Provisional Patent Application Serial No. 60/478,922, filed June 16, 2003, both of which are incorporated herein by reference for all
5 purposes.

BACKGROUND

1. Technical Field

The present invention relates generally to cellular wireless communication systems; and more particularly to the processing of data communications received by a wireless terminal in
10 such a cellular wireless communication system.

2. Related Art

Cellular wireless communication systems support wireless communication services in many populated areas of the world. While cellular wireless communication systems were initially constructed to service voice communications, they are now called upon to support data
15 communications as well. The demand for data communication services has exploded with the acceptance and widespread use of the Internet. While data communications have historically been serviced via wired connections, cellular wireless users now demand that their wireless units also support data communications. Many wireless subscribers now expect to be able to

“surf” the Internet, access their email, and perform other data communication activities using their cellular phones, wireless personal data assistants, wirelessly linked notebook computers, and/or other wireless devices. The demand for wireless communication system data communications will only increase with time. Thus, cellular wireless communication systems are currently being created/modified to service these burgeoning data communication demands.

Cellular wireless networks include a “network infrastructure” that wirelessly communicates with wireless terminals within a respective service coverage area. The network infrastructure typically includes a plurality of base stations dispersed throughout the service coverage area, each of which supports wireless communications within a respective cell (or set of sectors). The base stations couple to base station controllers (BSCs), with each BSC serving a plurality of base stations. Each BSC couples to a mobile switching center (MSC). Each BSC also typically directly or indirectly couples to the Internet.

In operation, each base station communicates with a plurality of wireless terminals operating in its cell/sectors. A BSC coupled to the base station routes voice communications between the MSC and a serving base station. The MSC routes voice communications to another MSC or to the PSTN. Typically, BSCs route data communications between a servicing base station and a packet data network that may include or couple to the Internet. Transmissions from base stations to wireless terminals are referred to as “forward link” transmissions while transmissions from wireless terminals to base stations are referred to as “reverse link” transmissions. The volume of data transmitted on the forward link typically exceeds the volume of data transmitted on the reverse link. Such is the case because data users typically issue commands to request data from data sources, e.g., web servers, and the web servers provide the data to the wireless terminals.

Wireless links between base stations and their serviced wireless terminals typically operate according to one (or more) of a plurality of operating standards. These operating standards define the manner in which the wireless link may be allocated, setup, serviced and torn down. One popular cellular standard is the Global System for Mobile telecommunications (GSM) standard. The GSM standard, or simply GSM, is predominant in Europe and is in use around the globe. While GSM originally serviced only voice communications, it has been modified to also service data communications. GSM General Packet Radio Service (GPRS) operations and the Enhanced Data rates for GSM (or Global) Evolution (EDGE) operations coexist with GSM by sharing the channel bandwidth, slot structure, and slot timing of the GSM standard. GPRS operations and EDGE operations may also serve as migration paths for other standards as well, e.g., IS-136 and Pacific Digital Cellular (PDC).

In order for EDGE to provide increased data rates within a 200 KHz GSM channel, it employs a higher order modulation, 8-PSK (octal phase shift keying), in addition to GSM's standard Gaussian Minimum Shift Keying (GMSK) modulation. EDGE allows for nine different (autonomously and rapidly selectable) air interface formats, known as Modulation and Coding schemes (MCSs), with varying degrees of error control protection. Low MCS modes, (MCS 1-4) use GMSK (low data rate) while high MCS modes (MCS 5-9) use 8-PSK (high data rate) modulation for over the air transmissions, depending upon the instantaneous demands of the application and the operating conditions.

EDGE uses the higher order 8-PSK and the GMSK modulations and a family of MCSs for each GSM radio channel time slot, so that each user connection may adaptively determine the best MCS setting for the particular radio propagation conditions and data access requirements of the user. In addition, the "best" air interface mode is enhanced with a technique called incremental redundancy (IR), whereby packets are transmitted first with

initially selected MCS mode and puncturing, and then subsequent packets are transmitted with additional redundancy using differing puncturing patterns and potentially different MCS modes within a common MCS family. Rapid feedback between the base station and wireless terminal may restore the previous acceptable air interface state, which is presumably at an acceptable level but with minimum required coding and with minimum bandwidth and power drain.

The GSM standard specifies communications in a time divided format (in multiple channels). The GSM standard specifies a 20 ms frame that is divided into four sub-frames, each including eight slots of approximately 625 μ s in duration. Each slot corresponds to a Radio Frequency (RF) burst having a left side, a midamble, and a right side.

A wireless terminal operating within a GSM system may require significant forward link (and/or reverse link) throughput during any given time period(s). To satisfy the forward link throughput requirements, the GSM network may allocate multiple forward link time slots to the wireless terminal. So that reverse link transmissions may be serviced in other of the slots, assigned slots that carry forward link transmissions are often adjacent one another, e.g., two or more time adjacent slots. The assignment of adjacent slots for forward link transmissions allows the wireless terminal to switch between transmit and receive operations within a single GSM frame/sub-frame.

Conventional wireless terminals have difficulty in receiving and processing RF bursts in adjacent slots and also meeting their other requirements. Thus, there exists a need for a wireless terminal that can receive and process multiple RF bursts while meeting the other requirements of the wireless terminal.

BRIEF SUMMARY OF THE INVENTION

In order to overcome these shortcomings of the prior devices, among others, a wireless

communication device processes N Radio Frequency (RF) bursts contained within N slots of a digital communications time divided frame, wherein N is a positive integer greater than one. The wireless communication device includes an RF front end, a baseband processor, and an equalizer module. The RF front end is operable to receive the plurality of received RF bursts
5 and to convert the RF bursts to corresponding baseband signals. The baseband processor operably couples to the RF front end, is operable to receive the baseband signals, is operable to pre-equalization process the baseband signals to produce processed baseband signals, and is operable to post-equalization process soft decisions. The equalizer module operably couples to the baseband processor and is operable to equalize the processed baseband signals to produce
10 the soft decisions.

According to the present invention, the baseband processor and the equalizer module are operable as a pipeline. With these pipeline operations, for at least one of the N RF bursts, the baseband processor performs pre-equalization processing of a corresponding baseband signal to produce a processed baseband signal while the equalizer module concurrently equalizes a
15 processed baseband signal corresponding to a prior RF burst to produce soft decisions. According to another aspect of these pipeline operations, for at least one of the N RF bursts, the baseband processor performs post-equalization processing of soft decisions corresponding to a prior RF burst while concurrently equalizing a processed baseband signal corresponding to the RF burst. These RF bursts may be contained in adjacent slots or, in non-adjacent slots, or in a
20 combination of adjacent slots and non-adjacent slots.

Other features and advantages of the present invention will become apparent from the following detailed description of the invention made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a system diagram illustrating a portion of a cellular wireless communication system that supports wireless terminals operating according to the present invention;

FIG. 2 is a block diagram functionally illustrating a wireless terminal constructed
5 according to the present invention;

FIG. 3 is a block diagram illustrating in more detail the wireless terminal of FIG. 2, with particular emphasis on the digital processing components of the wireless terminal;

FIG. 4 is a block diagram illustrating the general structure of a GSM frame and the manner in which data blocks are carried by the GSM frame;

10 FIG. 5 is a block diagram illustrating the manner in which a wireless terminal may be allocated a plurality of slots in a GSM frame;

FIGs. 6A and 6B are flow charts illustrating operation of a wireless terminal in receiving and processing a RF burst;

15 FIG. 7 is a flow chart illustrating operations of the baseband processor according to an embodiment of the present invention; and

FIG. 8 is a block diagram illustrating pipeline processing operations performed according to the present invention.

DETAILED DESCRIPTION OF THE DRAWINGS

20 FIG. 1 is a system diagram illustrating a portion of a cellular wireless communication system 100 that supports wireless terminals operating according to the present invention. The cellular wireless communication system 100 includes a Mobile Switching Center (MSC) 101, Serving GPRS Support Node/Serving EDGE Support Node (SGSN/SESN) 102, base station controllers (BSCs) 152 and 154, and base stations 103, 104, 105, and 106. The SGSN/SESN

102 couples to the Internet 114 via a GPRS Gateway Support Node (GGSN) 112. A conventional voice terminal 121 couples to the PSTN 110. A Voice over Internet Protocol (VoIP) terminal 123 and a personal computer 125 couple to the Internet 114. The MSC 101 couples to the Public Switched Telephone Network (PSTN) 110.

5 Each of the base stations 103-106 services a cell/set of sectors within which it supports wireless communications. Wireless links that include both forward link components and reverse link components support wireless communications between the base stations and their serviced wireless terminals. These wireless links support digital data communications, VoIP communications, and other digital multimedia communications. The cellular wireless
10 communication system 100 may also be backward compatible in supporting analog operations as well. The cellular wireless communication system 100 supports the Global System for Mobile telecommunications (GSM) standard and also the Enhanced Data rates for GSM (or Global) Evolution (EDGE) extension thereof. The cellular wireless communication system 100 may also support the GSM General Packet Radio Service (GPRS) extension to GSM.
15 However, the present invention is also applicable to other standards as well, e.g., TDMA standards, CDMA standards, etc. In general, the teachings of the present invention apply to digital communications that combine Automatic Repeat ReQuest (ARQ) operations at Layer 2, e.g., LINK/MAC layer with variable coding/decoding operations at Layer 1 (PHY).

Wireless terminals 116, 118, 120, 122, 124, 126, 128, and 130 couple to the cellular
20 wireless communication system 100 via wireless links with the base stations 103-106. As illustrated, wireless terminals may include cellular telephones 116 and 118, laptop computers 120 and 122, desktop computers 124 and 126, and data terminals 128 and 130. However, the cellular wireless communication system 100 supports communications with other types of wireless terminals as well. As is generally known, devices such as laptop computers 120 and

122, desktop computers 124 and 126, data terminals 128 and 130, and cellular telephones 116 and 118, are enabled to “surf” the Internet 114, transmit and receive data communications such as email, transmit and receive files, and to perform other data operations. Many of these data operations have significant download data-rate requirements while the upload data-rate requirements are not as severe. Some or all of the wireless terminals 116-130 are therefore enabled to support the GPRS and/or EDGE operating standard as well as supporting the voice servicing portions the GSM standard.

In particular, the wireless terminals 116-130 support the pipelined processing of received RF bursts in slots of a GSM frame so that a plurality of slots in each sub-frame of a GSM frame are allocated for forward link transmissions to a single wireless terminal. In one particular embodiment, a number of slots of a GSM frame are allocated for forward link transmissions to a wireless terminal such that the wireless terminal must receive and process a number of RF bursts, e.g., 2, 3, 4, or more RF bursts, in each sub-frame of the GSM frame. The wireless terminal is able to process the RF bursts contained in these slots and still service reverse link transmissions and the other processing requirements of the wireless terminal.

FIG. 2 is a block diagram functionally illustrating a wireless terminal 200 constructed according to the present invention. The wireless terminal 200 of FIG. 2 includes an RF transceiver 202, digital processing components 204, and various other components contained within a housing. The digital processing components 204 includes two main functional components, a physical layer processing, speech COder/DECoder (CODEC), and baseband CODEC functional block 206 and a protocol processing, man-machine interface functional block 208. A Digital Signal Processor (DSP) is the major component of the physical layer processing, speech COder/DECoder (CODEC), and baseband CODEC functional block 206 while a microprocessor, e.g., Reduced Instruction Set Computing (RISC) processor, is the

major component of the protocol processing, man-machine interface functional block 208. The DSP may also be referred to as a Radio Interface Processor (RIP) while the RISC processor may be referred to as a system processor. However, these naming conventions are not to be taken as limiting the functions of these components.

5 The RF transceiver 202 couples to an antenna 203, to the digital processing components 204, and also to a battery 224 that powers all components of the wireless terminal 200. The physical layer processing, speech Coder/DECoder (CODEC), and baseband CODEC functional block 206 couples to the protocol processing, man-machine interface functional block 208 and to a coupled microphone 226 and speaker 228. The protocol processing, man-machine
10 interface functional block 208 couples to a Personal Computing/Data Terminal Equipment interface 210, a keypad 212, a Subscriber Identification Module (SIM) port 213, a camera 214, a flash RAM 216, an SRAM 218, a LCD 220, and LED(s) 222. The camera 214 and LCD 220 may support either/both still pictures and moving pictures. Thus, the wireless terminal 200 of FIG. 2 supports video services as well as audio services via the cellular network.

15 FIG. 3 is a block diagram illustrating in more detail the wireless terminal of FIG. 2, with particular emphasis on the digital processing components of the wireless terminal. The digital processing components 204 include a system processor 302, a baseband processor 304, and a plurality of supporting components. The supporting components include an external memory interface 306, MMI drivers and I/F 308, a video I/F 310, an audio I/F 312, a voice band
20 CODEC 314, auxiliary functions 316, a modulator/demodulator 322, ROM 324, RAM 326 and a plurality of processing modules. In some embodiments, the modulator/demodulator 322 is not a separate structural component with these functions being performed internal to the baseband processor 304.

The processing modules are also referred to herein as accelerators, co-processors,

processing modules, or otherwise, and include auxiliary functions 316, an equalizer module 318, an encoder/decoder module 320, and an Incremental Redundancy (IR) processing module 328. The interconnections of FIG. 3 are one example of a manner in which these components may be interconnected. Other embodiments support additional/alternate couplings. Such coupling may be direct, indirect, and/or may be via one or more intermediary components.

RAM and ROM service both the system processor 302 and the baseband processor 304. Both the system processor 302 and the baseband processor 304 may couple to shared RAM 326 and ROM 324, couple to separate RAM, coupled to separate ROM, couple to multiple RAM blocks, some shared, some not shared, or may be served in a differing manner by the memory.

In one particular embodiment, the system processor 302 and the baseband processor 304 coupled to respective separate RAMs and ROMs and also couple to a shared RAM that services control and data transfers between the devices. The processing modules 316, 318, 320, 322, and 328 may coupled as illustrated in FIG. 3 but may also coupled in other manners in differing embodiments.

The system processor 302 services at least a portion of a serviced protocol stack, e.g., GSM/GPRS/EDGE protocol stack. In particular the system processor 302 services Layer 1 (L1) operations 330, a portion of Incremental Redundancy (IR) GSM protocol stack operations 332 (referred to as "IR control process"), Medium Access Control (MAC) operations 334, and Radio Link Control (RLC) operations 336. The baseband processor 304 in combination with the modulator/demodulator 322, RF transceiver, equalizer module 318, and/or encoder/decoder module 320 service the Physical Layer (PHY) operations performed by the digital processing components 204.

Still referring to FIG. 3, the baseband processor 304 implements a pipeline processing control function 338 that controls the interaction of the baseband processor 304 and equalizer

module 318. As will be described further with reference to FIGs. 5-8, the pipeline processing control function 338 implemented by the baseband processor 304 is responsible for causing the equalizer module 318 and baseband processor 304 to pipeline process received RF bursts that reside within slots of a GSM frame. In the particular embodiment of FIGs. 2 and 3, with the single RF front end 202, the wireless terminal 200 may receive and process RF bursts in up to four slots of each sub-frame of a GSM frame, i.e., be assigned four slots for forward link transmissions in any particular GSM frame. In another embodiment in which the wireless terminal 200 includes more than one RF front end, the wireless terminal 200 may be assigned more than four slots in each sub-frame of the GSM frame. In this case, required transmit operations would be performed using a second RF front end while a first RF front end would perform the receive operations. When the forward link transmissions and the reverse link transmissions occupy different channels with sufficient frequency separation, and the wireless terminal otherwise supports full duplex operations, the wireless terminal could receive and transmit at the same time.

FIG. 4 is a block diagram illustrating the general structure of a GSM frame and the manner in which data blocks are carried by the GSM frame. The GSM frame is 20 ms in duration, including guard periods, is divided into four sub-frames, and includes eight slots, slots 0 through 7, in each sub-frame. Each slot is approximately 577 μ s in duration, includes a left side, a midamble, and a right side. The left side and right side of an RF burst of the time slot carry data while the midamble is a training sequence.

The RF bursts of four time slots of the GSM frame carry a segmented RLC block, a complete RLC block, or two RLC blocks, depending upon a supported Modulation and Coding Scheme (MCS) mode. For example, data block A is carried in slot 0 of sub-frame 1, slot 0 of sub-frame 2, slot 0 of sub-frame 3, and slot 0 of sub-frame 3. Data block A may carry a

segmented RLC block, an RLC block, or two RLC blocks. Likewise, data block B is carried in slot 1 of sub-frame 1, slot 1 of sub-frame 2, slot 1 of sub-frame 3, and slot 1 of sub-frame 3. The MCS mode of each set of slots, i.e., slot n of each sub-frame, for the GSM frame is consistent for the GSM frame. Further, the MCS mode of differing sets of slots of the GSM frame, e.g., slot 0 of each sub-frame vs. any of slots 1-7 of each sub-frame, may differ. As will be described further with reference to FIG. 5, the wireless terminal 200 may be assigned multiple slots for forward link transmissions that must be received and processed by the wireless terminal 200.

FIG. 5 is a block diagram illustrating the manner in which a wireless terminal 200 may be allocated a plurality of slots in a GSM frame. Shown in FIG. 5 is a portion of the GSM frame previously fully illustrated in FIG. 4. In the embodiment of FIG 5, the wireless terminal 200 is allocated slots 0-3 of each GSM sub-frame for forward link transmissions. Thus, the wireless terminal 200 performs receive operations for each of slots 0-3 of each GSM sub-frame. Complimentary to the receive operation are transmit operations in slots 5-6 of each GSM sub-frame. Because of the construct of a typical wireless terminal, e.g., wireless terminal 200 of FIG. 2, a single RF front end 202 services both receive operations and transmit operations but can operate only in one of a receive mode and a transmit mode at any time. Thus, the wireless terminal 200 must quickly switch from the receive mode to the transmit mode to service reverse link communications. In the example of FIG. 5, the wireless terminal 200 transitions during slot 4 from receive operations for slots 0-3 to transmit operations for slots 5-6, and transitions during slot 7 back to receive operations for slots 0-3 of the next sub-frame. A wireless terminal having multiple RF front ends may service both receive operations and transmit operations concurrently on differing channels and, absent prohibitive interference, the wireless terminal could be assigned all eight slots for forward link transmissions. When concurrent transmit and

receive operations are prohibited, the multiple RF front ends would allow the wireless terminal to transmit and receive in adjacent frames, without requiring the intervening idle slot.

With the pipeline processing capabilities of the wireless terminal 200 of the present invention, the wireless terminal 200 is capable of receiving and processing forward link transmissions in slots 0-3. As will be described further with reference to FIGs. 6A-8, the baseband processor 304 and the equalizer module 318 execute pipeline processing operations on received RF bursts. These operations may be easily applied to any number of RF bursts contained in a corresponding number of assigned slots.

While FIG. 5 shows an allocation of slots 0-3 for receive operations and slots 5-6 for transmit operations, such an allocation is not required by the present invention. With one alternate operation shown, receive operations are performed for slots 2-5 of each GSM sub-frame while transmit operations are performed for slot 7 and slot 0 of each sub-frame. In the embodiment, slots 1 and 6 are used for switching between transmit and receive operations. Further, the allocated forward link slots and/or allocated reverse link slots need not be adjacent one another. For example, the wireless terminal could be assigned forward link transmissions in slots 1, 2, and 4 and reverse link operations in slot 6. Moreover, for a wireless terminal having two RF front ends, the idle slots illustrated in FIG. 5 would not be required and such slots could be allocated for forward link transmissions (or reverse link transmissions). As the reader will appreciate, many differing allocations may be made without departing from the scope of the present invention.

FIGs. 6A and 6B are flow charts illustrating operation of a wireless terminal 200 in receiving and processing a RF burst. The operations illustrated in FIG. 6A to 6B correspond to a single RF burst in a corresponding slot of GSM frame. At least the RF front end 202, the baseband processor 304, and the equalizer module 318 illustrated in FIG. 3 perform these

operations. These operations are generally called out as being performed by one of these components. However, the split of processing duties among these various components may differ without departing from the scope of the present invention.

Referring particular to FIG. 6A, operation commences with the RF front end 202 receiving an RF burst in a corresponding slot of a GSM frame (step 602). The RF front end 202 then converts the RF burst to a baseband signal (step 604). Upon completion of the conversion, the RF front end 202 sends an interrupt to the baseband processor 304 (step 606). Thus, as referred to in FIG. 6A, steps 602-606 are performed by the RF front end 202.

Operation continues with the baseband processor 304 receiving the baseband signal (step 608). In a typical operation, either the RF front end 202, the baseband processor 304, or modulator/demodulator 322 will sample the analog baseband signal to digitize the baseband signal. After receipt of the baseband signal (in a digitized format), the baseband processor 304 performs blind detection of a modulation format of the baseband signal (step 610). This blind detection of the modulation format determines the modulation format of the corresponding baseband signal. In one particular embodiment according to the GSM standard, the modulation format will be either Gaussian Minimum Shift Keying (GMSK) modulation or Eight Phase Shift Keying (8PSK) modulation. The baseband processor 304 makes the determination (step 612) and proceeds along one of two branches based upon the detected modulation format.

For GMSK modulation, the baseband processor 304 performs de-rotation and frequency correction of the baseband signal (step 614). Next, the baseband processor 304 performs burst power estimation of the baseband signal (step 616). Referring now to FIG. 6B via off page connector A, the baseband processor 304 next performs timing, channel, noise, and signal-to-noise ratio (SNR) estimation (step 620). Subsequently, the baseband processor 304 performs automatic gain control (AGC) loop calculations (step 622). Next, the baseband processor 304

performs soft decision scaling factor determination on the baseband signal (step 624). After step 624, the baseband processor 304 performs matched filtering operations on the baseband signal (step 626).

Steps 608-626 are referred to hereinafter as pre-equalization processing operations.

5 With the baseband processor 304 performing these pre-equalization processing operations on the baseband signal it produces a processed baseband signal. Upon completion of these pre-equalization processing operations, the baseband processor 304 issues a command to the equalizer module 318.

The equalizer module 318, upon receiving the command, prepares to equalize the
10 processed baseband signal based upon the modulation format, e.g., GMSK modulation or 8PSK modulation. The equalizer module 318 receives the processed baseband signal, settings, and/or parameters from the baseband processor 304 and performs Maximum Likelihood Sequence Estimation (MLSE) equalization on the left side of the baseband signal (step 628). As was shown previously with reference to FIG. 4, each RF burst contains a left side of data, a
15 midamble, and a right side of data. At step 628, the equalizer module 318 equalizes the left side of the RF burst to produce soft decisions for the left side. Then, the equalizer module 318 equalizes the right side of the processed baseband signal (step 630). The equalization of the right side produces a plurality of soft decisions corresponding to the right side.

The equalizer module 318 then issues an interrupt to the baseband processor 304
20 indicating that the equalizer operations are complete for the RF burst. The baseband processor 304 then receives the soft decisions from the equalizer module 318. Next, the baseband processor 304 determines an average phase of the left and right sides based upon the soft decisions received from the equalizer module 318 (step 632). The baseband processor 304 then performs frequency estimation and tracking based upon the soft decisions received from the

equalizer module 318 (step 636). The operations of step 632 (or step 654) and step 636 are referred to herein as “post-equalization processing.” After operation at step 636, processing of the particular RF burst is completed.

Referring again to FIG. 6A, the baseband processor 304 and equalizer module 318 take the right branch from step 612 when an 8PSK modulation is blindly detected at step 610. In the first operation for 8PSK modulation, the baseband processor 304 performs de-rotation and frequency correction on the baseband signal (step 618). The baseband processor 304 then performs burst power estimation of the baseband signal (step 620). Referring now to FIG. 6B via off page connector B, operation continues with the baseband processor 304 performing timing, channel, noise, and SNR estimations (step 640). The baseband processor 304 then performs AGC loop calculations on the baseband signal (step 642). Next, the baseband processor 304 calculates Decision Feedback Equalizer (DFE) coefficients that will be used by the equalizer module 318 (step 644). The baseband processor 304 then performs pre-equalizer operations on the baseband signal (step 646). Finally, the baseband processor 304 determines soft decision scaling factors for the baseband signal (step 648). Steps 618-648 performed by the baseband processor 304 are referred to herein as “pre-equalization processing” operations for an 8PSK modulation baseband signal. Upon completion of step 648, the baseband processor 304 issues a command to equalizer module 318 to equalize the processed baseband signal.

Upon receipt of the command from the baseband processor 304, the equalizer module 318 receives the processed baseband signal, settings, and/or parameters from the baseband processor 304 and commences equalization of the processed baseband signal. The equalizer module 318 first prepares state values that it will use in equalizing the 8PSK modulated processed baseband signal (step 650). In the illustrated embodiment the equalizer module 318

uses a Maximum A posteriori Probability (MAP) equalizer . The equalizer module 318 then equalizes the left and right sides of the processed baseband signal using the MAP equalizer to produce soft decisions for the processed baseband signal (step 652). Upon completion of step 654, the equalizer module 318 issues an interrupt to the baseband processor 304 indicating its completion of equalizing the processed baseband signal corresponding.

The baseband processor 304 then receives the soft decisions from the equalizer module 318. Next, the baseband processor 304 determines the average phase of the left and right sides of the processed baseband signal based upon the soft decisions (step 654). Finally, the baseband processor 304 performs frequency estimation and tracking for the soft decisions (step 636). The operations of steps 654 and 636 are referred to as post-equalization processing operations. From step 636, operation is complete for the particular RF burst.

FIG. 7 is a flow chart illustrating operations of the baseband processor 302 according to an embodiment of the present invention. Operation commences wherein the baseband processor is either idle or performing operations not specified in FIG. 7 (step 702). The baseband processor 304 receives an Rx interrupt from the RF front end 202 for an RF burst contained in a corresponding time slot (step 704). When the baseband processor is ready (step 706), it receives a baseband signal corresponding to the RF burst from the RF front end 202 (step 708). The baseband processor 304 receives a digitized signal from the RF front end 202 or intermediary component such as the modulator/demodulator 322 shown in FIG. 3.

The baseband processor 304 then performs pre-equalization processing on the baseband signal (step 710). The pre-equalization processing performed by the baseband processor 304 was described in detail with reference to FIGs. 6A and 6B. Such pre-equalization processing differs for the different modulation formats supported by the wireless terminal 200. The baseband processor 304 then determines equalizer settings/parameters that will be employed by

the equalizer module 318 (step 712). Then, the baseband processor 304 sends a command to the equalizer module 318 directing the equalizer module 318 to equalize the processed baseband signal (step 714). With the equalizer module 318 responding to the command, the baseband processor 304 passes the processed baseband signal, the parameters, and the settings that were determined at step 712 to the equalizer module 318 (step 716).

Steps 704-716 describe the pre-equalization processing operations performed by the baseband processor 304 on a particular RF burst. As will be further described with reference to FIG. 8, the baseband processor 304 performs pre-equalization processing on the baseband signal and passes the processed baseband signal (and equalizer settings/parameters in some embodiments) to the equalizer module 318. While the equalizer module 318 is equalizing the processed baseband signal for a corresponding RF burst, the baseband processor 304 performs pre-equalization processing on a baseband signal corresponding to a subsequent RF burst. After the equalizer module 318 has completed its equalization of the baseband signal to produce soft decisions, the baseband processor 304 performs post-equalization processing on the soft decisions returned by the equalizer module 318.

The post-equalization operations of the baseband processor 304 commence with the baseband processor 304 receiving an interrupt from the equalizer module 318 (step 718). Upon receipt of the interrupt from the equalizer module 318, the baseband processor 304 may not be able to immediately service the interrupt because of its performing pre-equalization processing operations on a baseband signal corresponding to a subsequent RF burst. When the baseband processor 304 is ready to process (step 720), the baseband processor 304 receives the soft decisions from the equalizer module 318 (step 722). Then, the baseband processor 304 performs post-equalization processing on the soft decisions received from the equalizer module 318 (step 724). With the post-equalization operations on the plurality of soft decisions

completed, the baseband processor stores the plurality of soft decisions for subsequent use (step 726).

After the processing a complete GSM frame, 4 sets of soft decisions corresponding to a data block, e.g., segmented RLC data block, RLC block, or multiple RLC blocks, the baseband processor 304 is ready for subsequent processing. When this determination is made at step 728, the baseband processor 304 retrieves the post-equalization processed soft decisions for the data block (step 730). Four sets of processed soft decisions correspond to either a segmented RLC block, a complete RLC block, or two RLC blocks. The baseband processor 304 then passes the data block soft decisions to the encoder/decoder module 320 or to the system processor 302 depending upon the type of data block. For example, encoder/decoder module 320 performs decoding operations on GSM voice data blocks and GPRS data blocks while IR processing module 328 performs encoding/decoding operations on EDGE data blocks. From steps 716, 726 and 732 operation returns to step 702.

FIG. 8 is a block diagram illustrating pipeline processing operations performed according to the present invention. Particularly, FIG. 8 is intended to illustrate how a wireless terminal receives and processes multiple RF bursts in a pipelined fashion. With the example of FIG. 8, slots 0-3 service forward link transmissions for the wireless terminal 200. In a first operation, the RF front end 202 receives an RF burst in slot 0 and issues an interrupt to the baseband processor 304 after reception is complete. Upon receipt of the interrupt, the baseband processor 304 receives the baseband signal corresponding to the RF burst of slot 0 from the RF front end 202 and performs pre-equalization processing of the baseband signal. Resultantly, the baseband processor 304 produces a processed baseband signal and upon completion issues a baseband processor command to the equalizer module 318 that corresponds to slot 0 RF burst.

The equalizer module 318 receives the processed baseband signal from the baseband

processor 304. The equalizer module 318 then equalizes the processed baseband signal corresponding to slot 0 and, upon completion, issues an equalizer module interrupt to the baseband processor 304. As is shown in FIG. 8, with time progressing from left to right, when the equalizer module 318 completes its processing of the baseband signal corresponding to slot 0, the RF front end 202 has already issued an interrupt to the baseband processor 304, the baseband processor 304 has already received the baseband signal, and the baseband processor 304 is already performing pre-equalization processing on the baseband signal corresponding to slot 1. Thus, while the equalizer module 318 is equalizing the processed baseband signal corresponding to slot 0, the baseband processor 304 is performing pre-equalization processing on the baseband signal corresponding to slot 1. The pipeline processing supported by the components of the wireless terminal 200 allows it to receive and process RF bursts in adjacent slots.

Once the baseband processor 304 has completed its pre-equalization processing on the baseband signal corresponding to slot 1, it issues a command to the equalizer module 318 for the processed baseband signal corresponding to slot 1. Then, the baseband processor 304 services the interrupt received from the equalizer module 318 corresponding to slot 0 by receiving the soft decisions corresponding to slot 0, and by performing post-equalization processing on the plurality of soft decisions corresponding to slot 0.

Pipeline processing operations continue for slots 1 and 2 and partially for slot 3 as are illustrated in FIG 8. However, upon completion of equalization of the processed baseband signal corresponding to slot 3 by the equalizer module 318, the baseband processor 304 may be idle and be awaiting the interrupt from the equalizer module 318. Once the equalizer module 318 issues an interrupt to the baseband processor 304, the baseband processor receives the soft decisions from the equalizer module 318 and performs post-equalization processing on the

plurality of soft decisions corresponding to slot 3. The operations of FIG. 8 may be applied to fewer or more than four slots per sub-frame, a maximum number of slots supportable depending upon the supporting capabilities of the wireless terminal, e.g., multiple RF front ends, etc.

5 The foregoing description of a preferred embodiment of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and modifications and variations are possible in light of the above teachings or may be acquired from practice of the invention. The embodiment was chosen and described in order to explain the principles of the invention and its
10 practical application to enable one skilled in the art to utilize the invention in various embodiments and with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the claims appended hereto, and their equivalents.